

## Product Change Notification (PCN)

PCN no.: <b>PCN-082 1.0</b>		Date: <b>2013-10-28</b>
Device affected:		Device version / Build Code:
nRF51822-QFAA		CA, C0
nRF51822-QFAB		AA, A0
nRF51822-CEAA		BA, B0
Data sheet references: <b>See Appendix 1</b>	Agreement reference: <b>N/A</b>	Customers reference: <b>N/A</b>

**Description of change:**

New revision of the IC with the following key changes.

**Fixes of anomalies**  
 The new IC revision includes a number of fixes and improvements of anomalies reported in PAN-028. PAN-028 is now replaced by nRF51822-PAN v2.0 which includes an updated list of anomalies for all IC revisions.

**New features and changes in electrical specifications**  
 All new features and changes in electrical specifications for this new IC revision are documented in the *nRF51822 Product Specification* version 2.0 and the *nRF51 Reference Manual* version 2.0. Appendix 1 lists all changes with reference to these documents.

**Reduced radio local oscillator (LO) spurious emissions**  
 The new IC revision also includes design adjustments which reduce radio LO spurious emission levels for designs based on a discrete matching network.

**Impact:** Does the change affect product:

1. Form	<input checked="" type="checkbox"/> No	<input type="checkbox"/> Yes – describe:
2. Fit	<input checked="" type="checkbox"/> No	<input type="checkbox"/> Yes – describe:
3. Function	<input type="checkbox"/> No	<input checked="" type="checkbox"/> Yes – describe: Added/changed features, see Appendix 1
4. Quality or Reliability	<input checked="" type="checkbox"/> No	<input type="checkbox"/> Yes – describe:
Classification of change	<input type="checkbox"/> Minor	<input checked="" type="checkbox"/> Major

**Reason for change:**

Fixed anomalies in affected devices and addition of new features.

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### Consequences of change:

#### Hardware

The new device versions are drop-in compatible with the current versions, but note the following:

- External pull-down resistor on SWDCLK pin is no longer mandatory.
- Designs based on nRF51822-QFAA/nRF51822-QFAB combined with ST Microelectronics balun, BAL-NRF01D3 (as described in the reference layout *nRF51822-DF-ST v1.0*), are likely to fail Korean teleregulatory spurious emission limits due to LO leakage.

#### Software:

The new device versions are software compatible with the current revision for application code, but note the following:

- New IC revisions are only compatible with SoftDevice S110 v5.2 or later.
- Only nRF51 SDK v4.3.0 or later is tested with the new IC revisions.
- Customers using the NRF\_1MBIT radio mode and wanting to qualify the product in accordance with 47 CFR Part 15.247 are required to update the stack to handle copying of FICR override parameters to RADIO. The *nRF51 Series Reference Manual v2.0* provides a description of FICR and RADIO override features. For questions or clarifications, please contact Nordic technical support.



#### Teleregulatory and *Bluetooth* certification

- Reference design *nRF51822-DF* passes all telecommunications regulatory bodies requirements with the stated product changes. A reassessment of design performance due to applicable telecommunications regulatory requirements is required for any product not identical to this reference design.
- Bluetooth QDID B020654 is valid for the new device version. Bluetooth RF PHY conformance reassessment is recommended for all designs not identical to this QDID reference design.

#### Verification:

New device version will be approved and qualified under standard Nordic Semiconductor ASA QA procedures.

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<b>Marking/Shipping labels:</b>	
New device versions will be marked with new build codes as follows:	
<b>nRF51822-QFAA</b>	
Engineering release: build code FA, GC	
Production release: build code G0	
<b>nRF51822-QFAB</b>	
Production release: build code B0	
<b>nRF51822-CEAA</b>	
Engineering release: build code CA, DA	
Production release: build code D0	
<b>Change active from (date):</b>	<b>Change active from (lot no/date code):</b>
<b>Standard 90 day's notice for change</b>	N/A (See build code above)
Nordic provides <i>90 day's notice for the change from the day production quality samples and qualification reports are available for the new device versions.</i> Schedule is as follows:	
<i>Variant / Samples &amp; reports / change active from</i>	
QFAA / Week of October 28 <sup>th</sup> 2013 / + 90 days	
QFAB / Week of November 18 <sup>th</sup> 2013 / + 90 days	
CEAA / Week of November 18 <sup>th</sup> 2013 / + 90 days	
<b>Early production ramp</b>	
Nordic can support a limited set of customers with production ramp and volume within the 90 day's notice period. Please contact Nordic sales for more information.	
<b>Last time order (date):</b>	<b>Final shipment date:</b>
<N/A>	<N/A>
<b>Attachments:</b> <input type="checkbox"/> No <input checked="" type="checkbox"/> Yes – Appendix 1	
<b>Authorization for Nordic Semiconductor</b>	
Product Manager	Date: 2013-10-28      Sign: 
Quality Director	Date: 2013-10-28      Sign: 

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## Appendix 1

### Product Changes

Module	nRF51822 PS v2.0 chapter	nRF51 Series Reference Manual v2.0 chapter	Part changed/ Added	Comment
SPIS	4.10	26	SPI Slave	New peripheral module.
LPCOMP	4.16	31	Low Power Comparator	New peripheral module.
FICR	-	6.1.1	Override parameters	Added description on how to handle the override parameter set in FICR.
		6.2.15	OVERRIDDEN	New register.
		6.2.16	NRF_1MBIT[n]	New register set for the NRF_1BIT mode.
		6.2.17	BLE_1MBIT[n]	New register set for the BLE_1BIT mode.
POWER	-	11.1.2	System OFF mode	LPCOMP is a new wakeup source from System OFF.
		11.2.1	RESETREAS	New reset source (bit 17 = LPCOMP).
PPI	3.5	15.1.1	Pre-Programmed channels	Channel 20-31 is a set of Pre-programmed channels.
		15.2.1	CHEN	Added control of channel 20..31.
		15.2.2	CHENSET	Added control of channel 20..31.
		15.2.3	CHENCLR	Added control of channel 20..31.
		15.2.6	CHG[n] (n=0..3)	Added control of channel 20..31.
MPU	3.3	8.1.5	NVM protection blocks	Added functionality to have runtime protection of memory blocks preventing unauthorized erasing and writing.
		8.2.3	PROTENSET0	New register to control the NVM protection mechanism.
		8.2.4	PROTENSET1	New register to control the NVM protection mechanism.
		8.2.5	DISABLEINDEBUG	New register to control the NVM protection mechanism.
UART	4.12	28	Universal Asynchronous Receiver/ Transmitter	Increased the receive buffer from 2 to 6 byte.
		28.5	Reception	<p>Changed the behavior of how the RTS line is handled. The UART will now deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO.</p> <p>Changed the behavior on STOPRX task. The UART is now capable of receiving data for a given period after the STOPRX task is triggered. In addition it will give a RXTO event when the receiving period has elapsed.</p>

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Module	nRF51822 PS v2.0 chapter	nRF51 Series Reference Manual v2.0 chapter	Part changed/ Added	Comment																															
			Receive buffer	Clarify how the receive buffer should be handled. The RXD register (receive buffer) can only be read when a RXDRDY event has been received, and the RXDRDY event must be cleared before the data is read.																															
		28.8 / 28.9.9	Parity configuration/ CONFIG	Changed the Reset value and how the parity is setup on the UART. Also, see anomaly 40 in nRF51822-PAN.																															
RADIO	4.1	16.1.14	Bit counter	Added new functionality in the radio. A simple counter has been added that can be configured to generate an event after a specific number of bits have been transmitted or received.																															
		16.1.15/ 16.2.30-31	Override registers	Describe how to handle the override registers, copying data from FICR to the radio override registers when using the radio in NRF_1MBIT or BLE_1MBIT mode.																															
		16.2.1	SHORTS	Added one new short: DISABLED_RSSISTOP.																															
LFCLK	3.6.3	12.1.3	Calibrating the 32.768 kHz RC oscillator	The 16MHz crystal oscillator must be started before LFCLK calibration by the use of TASKS_HFCLKSTART task.																															
TIMER	4.2	17	Timer/ Counter	Timer0 now supports bit modes 8,16,24, and 32. This will also affect the default bit mode.																															
				Timer 1 and 2 now support both bit mode 8 and 16.																															
SYSTEM	6	--	Absolute maximum rating (Table 14)	<b>Supply voltage</b> VDD Min: -0,3 V, Max: <b>+3.9 V</b>																															
SYSTEM	8	--	Electrical specifications																																
	8.1.2	--	Table 19	<table border="1"> <thead> <tr> <th>Symbol</th> <th>Old value</th> <th>New value</th> <th>Units</th> </tr> </thead> <tbody> <tr> <td>I<sub>X16M</sub></td> <td>400</td> <td>470</td> <td>µA</td> </tr> <tr> <td>I<sub>STBY,X16M</sub></td> <td>35</td> <td>25</td> <td>µA</td> </tr> </tbody> </table>	Symbol	Old value	New value	Units	I <sub>X16M</sub>	400	470	µA	I <sub>STBY,X16M</sub>	35	25	µA																			
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Module	nRF51822 PS v2.0 chapter	nRF51 Series Reference Manual v2.0 chapter	Part changed/ Added	Comment																			
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