nRF93M1 Hardware Design and Verification

Guideline

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NORDIC® SEMICONDUCTOR

Contents

Revision history

Date	Description
July 2026	First draft release

1 Introduction

This document provides guidelines for the hardware design and integration of the nRF93M1 *Long-Term Evolution (LTE)* Cat 1 bis module. These guidelines help to ensure the best electrical, mechanical, and thermal performance of nRF93M1. The guidelines are intended for Nordic Semiconductor's customers, especially system integrators and hardware engineers.

2 Design overview

This section provides an overview of the operating conditions of nRF93M1 and a pinout with a description of each pin.

A list of supported *LTE* Cat 1 bis bands can be found in nRF93M1 Preliminary Datasheet.

2.1 Operating conditions

This section describes the operating conditions that affect the performance and behavior of nRF93M1.

Temperature range

The optimal operating case temperature (T_C) of nRF93M1 ranges from –15°C to 55°C, achieving the best RF performance including output power transmission and receiver sensitivity.

The nRF93M1 transceiver remains regulatory compliant for case temperatures that range from –35°C to 75°C. It can remain compliant at temperatures up to 85°C for short periods of time. Operating at temperatures above 75°C can shorten the module's lifetime. Case temperature is typically the main cause for degradation in RF performance and current consumption, but other factors, such as supply voltage and signaling parameters, can contribute as well.

Case temperature is affected by the ambient temperature combined with nRF93M1's internal thermal dissipation originating from the transceiver activity.

Thermal protection

nRF93M1 has a built-in thermal protection mechanism to prevent the RF *Power Amplifier (PA)* from breaking down and to keep the *LTE* modem from operating beyond its specified temperature range. Designers should take into account that the nRF93M1 can heat up significantly during operation, depending on the level of transmitter activity.

To minimize heating during operation, ensure a good thermal exit from the ground pads of the nRF93M1 to the application board. Ground pads near the RF PA (pins 81 and 102) are critical for a good thermal connection to the PCB to achieve optimal thermal performance. It is also advised to use the lowest possible operating voltage level to minimize power dissipation.

When the internal temperature sensor in the nRF93M1 measures a case temperature of 100±5°C, the LTE modem is deactivated to minimize the internal heat generation and to protect the RF PA. The host *Microcontroller Unit (MCU)* can monitor case temperature using the **%ADC** AT command and **%PALARM** notifications. When **%PALARM** indicates that the case temperature has dropped below 85°C, the host can reactivate the LTE modem with the **+CFUN** AT command. The **AT+CFUN=1** command is disabled when the internal temperature sensor measures a case temperature greater than 85°C.

For more information on the commands used, see the nRF93M1 AT Commands reference guide.

Voltage range

The operational voltage of nRF93M1 can be found in the nRF93M1 Preliminary Datasheet. The LTE Cat 1 bis requires a minimum voltage of 3.3 V to fulfill RF performance in the environmental conditions described in the nRF93M1 Preliminary Datasheet. For optimal RF performance in LTE, a voltage of 3.5 V is recommended. This minimizes power dissipation while giving the RF PA optimal operating conditions.

Note: Minimum voltage includes all voltage drops, ripple, and spikes.

Undervoltage detection

nRF93M1 includes a built-in undervoltage protection mechanism that prevents operation of the LTE modem at certain voltage levels. If the internal voltage sensor measures a voltage below 2.8 V, the LTE modem is deactivated.

The internal voltage sensor also detects voltage ripple, which most commonly occurs during data transmission. For this reason, it is essential to follow the design guidelines for **VDD** to ensure stable operation. In addition, the **AT+CFUN=1** command is disabled whenever the module measures a **VDD** voltage below 3 V.

For regulatory compliance, the module's input voltage must be a minimum of 3.3 V. The host MCU can monitor the module's voltage using the **%ADC** AT command and **%PALARM** notifications.

See the nRF93M1 AT Commands reference guide for more information.

2.2 Physical characteristics

The nominal dimensions of nRF93M1 are 17.7x15.8x2.4 mm.

nRF93M1 has a fixed metal shield can to suppress internal radiated emissions and protect against external radio interference.

2.3 Pinout

This section describes the physical pin mapping and functions of the pins in nRF93M1.

There are 109 pins in nRF93M1. The pin assignment of nRF93M1 is shown in the following figure.

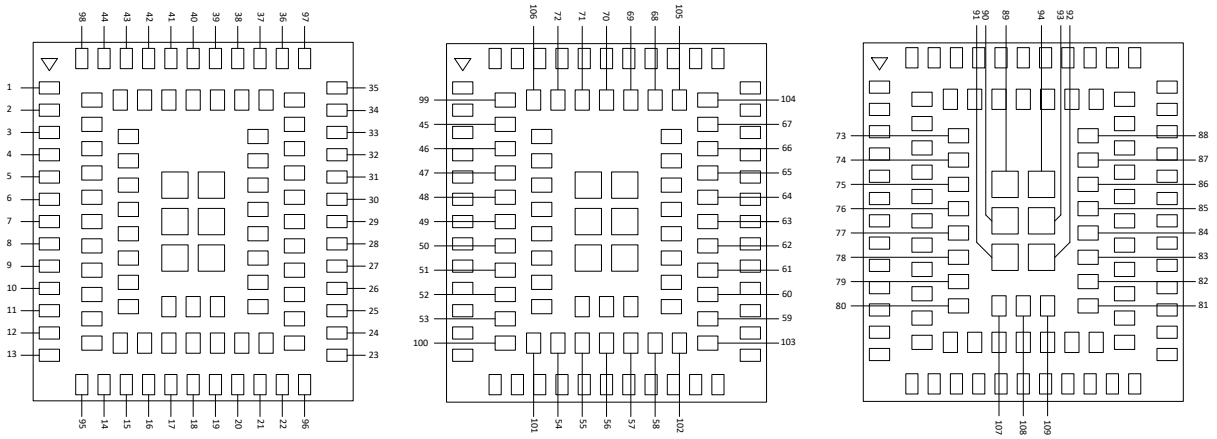

Figure 1: nRF93M1 pin assignment, top view

For more information, see nRF93M1 Preliminary Datasheet.

Pin description

Each nRF93M1 pin has specified functions and design recommendations. The detailed design recommendations are provided in Hardware integration on page 12.

The following table describes the functions of the nRF93M1 pins.

Pin no.	Pin name	Function	Description
1	**GND**	Power	Ground.

Pin no.	Pin name	Function	Description
2	GND	Power	Ground.
3	GND	Power	Ground.
4	GND	Power	Ground.
5	P0.0_AO	Digital I/O	Wake-up pin, always on, 1.8 V.
6	P0.1_AO	Digital I/O	RF Control interface, 1.8 V.
7	POWERKEY	System DISABLE	Enter or exit System DISABLE, active low.
8	GND	Power	Ground.
9	GND	Power	Ground.
10	GND	Power	Ground.
11	SIM1_IO	Digital I/O	SIM1 data.
12	SIM1_RST	Digital I/O	SIM1 reset.
13	SIM1_CLK	Digital I/O	SIM1 clock.
95	GND	Power	Ground.
14	SIM1_VOUT	Power	SIM power supply, 1.8 V or 3.0 V, auto detect based on type of SIM selected.
15	nRESET	Digital I/O	Module reset pin, 1.15 V, active low.
16	NETWORK	Digital I/O	Network status indicator, 1.8 V.
17	UART1_RXD	Digital I/O	UART1 Receive, 1.8 V.
18	UART1_TXD	Digital I/O	UART1 Transmit, 1.8 V.
19	UART1_DTR	Digital I/O	UART1 Data Terminal Ready, 1.8 V.
20	UART1_RI	Digital I/O	UART1 Ring Indicator, 1.8 V.
21	RESERVED		Connect thermally and mechanically to the application board but leave electrically unconnected.
22	UART1_RTS	Digital I/O	UART1 DTE Request Transmission, 1.8 V.
96	GND	Power	Ground.
23	UART1_CTS	Digital I/O	UART1 DTE Clear to Send, 1.8 V.
24	LDO_OUT	Power	LDO power out, nominal 1.8 V, max 120 mA.
25	STATUS	Digital I/O	Module operating status, 1.8 V.
26	GND	Power	Ground.
27	GND	Power	Ground.
28	UART2_RXD	Digital I/O	UART2 RX, 1.8 V.
29	UART2_TXD	Digital I/O	UART2 TX, 1.8 V.
30	GND	Power	Ground.
31	GND	Power	Ground.

Pin no.	Pin name	Function	Description
32	GND	Power	Ground.
33	GND	Power	Ground.
34	GND	Power	Ground.
35	ANT	RF	Single-ended 50 Ω LTE antenna pin.
97	GND	Power	Ground.
36	GND	Power	Ground.
37	GND	Power	Ground.
38	UART0_RXD	Digital I/O	UART0 RX, 1.8 V.
39	UART0_TXD	Digital I/O	UART0 TX, 1.8 V.
40	GND	Power	Ground.
41	GND	Power	Ground.
42	VDD	Power	nRF93M1's supply voltage input, 3.3 V to 4.5 V.
43	VDD	Power	nRF93M1's supply voltage input, 3.3 V to 4.5 V.
44	GND	Power	Ground.
98	GND	Power	Ground.
99	GND	Power	Ground.
45	GND	Power	Ground.
46	GND	Power	Ground.
47	GND	Power	Ground.
48	GND	Power	Ground.
49	GND	Power	Ground.
50	GND	Power	Ground.
51	GND	Power	Ground.
52	GND	Power	Ground.
53	GND	Power	Ground.
100	P0.2_AO	Digital I/O	RF Control interface, 1.8 V.
101	P0.3_AO	Digital I/O	RF Control interface, 1.8 V.
54	GND	Power	Ground.
55	GND	Power	Ground.
56	GND	Power	Ground.
57	RESERVED		Connect thermally and mechanically to the application board but leave electrically unconnected.

Pin no.	Pin name	Function	Description
58	**RESERVED**		Connect thermally and mechanically to the application board but leave electrically unconnected.
102	**GND**	Power	Ground.
103	**RESERVED**		Connect thermally and mechanically to the application board but leave electrically unconnected.
59	**USB_DP**	Digital I/O	USB differential data +.
60	**USB_DN**	Digital I/O	USB differential data -.
61	**USB_VBUS**	Digital I/O	USB VBUS input and system OFF wake-up.
62	**SIM2_CLK**	Digital I/O	SIM2 clock.
63	**SIM2_RST**	Digital I/O	SIM2 reset.
64	**SIM2_IO**	Digital I/O	SIM2 data.
65	**SIM2_VOUT**	Power	SIM power supply output, same net/voltage as **SIM1_VOUT**.
66	**UART2_RTS**	Digital I/O	UART2 DTE Request Transmission, 1.8 V.
67	**UART2_CTS**	Digital I/O	UART2 Clear to Send, 1.8 V.
104	**COEX0**	Digital I/O	Coexistence and RF Control interface, 1.8 V.
105	**COEX1**	Digital I/O	Coexistence and RF Control interface, 1.8 V.
68	**GND**	Power	Ground.
69	**GND**	Power	Ground.
70	**GND**	Power	Ground.
71	**GND**	Power	Ground.
72	**GND**	Power	Ground.
106	**GND**	Power	Ground.
73	**GND**	Power	Ground.
74	**GND**	Power	Ground.
75	**GND**	Power	Ground.
76	**GND**	Power	Ground.
77	**GND**	Power	Ground.
78	**GND**	Power	Ground.
79	**SIM1_DET**		SIM1 detect. If not used it must be left floating.
80	**GND**	Power	Ground.
107	**GND**	Power	Ground.
108	**GND**	Power	Ground.

Pin no.	Pin name	Function	Description
109	GND	Power	Ground.
81	GND	Power	Ground.
82	RESERVED		Connect thermally and mechanically to the application board but leave electrically unconnected.
83	GND	Power	Ground.
84	GND	Power	Ground.
85	GND	Power	Ground.
86	GND	Power	Ground.
87	GND	Power	Ground.
88	GND	Power	Ground.
89	GND	Power	Ground.
90	GND	Power	Ground.
91	GND	Power	Ground.
92	GND	Power	Ground.
93	GND	Power	Ground.
94	GND	Power	Ground.

Table 1: LGA pin assignments

3 Hardware integration

This section provides design recommendations, schematic drawings, and layout guidelines for each nRF93M1 pin for a successful integration of nRF93M1.

3.1 Schematic design

The schematic design should start by focusing on nRF93M1's most critical interfaces, which are the power supplies and the radio frequency interface.

Universal Integrated Circuit Card (UICC) and control interfaces should also be designed carefully, as these might need components for *Electrostatic Discharge (ESD)* protection or noise filtering. The following figure shows nRF93M1 schematic with recommended components.

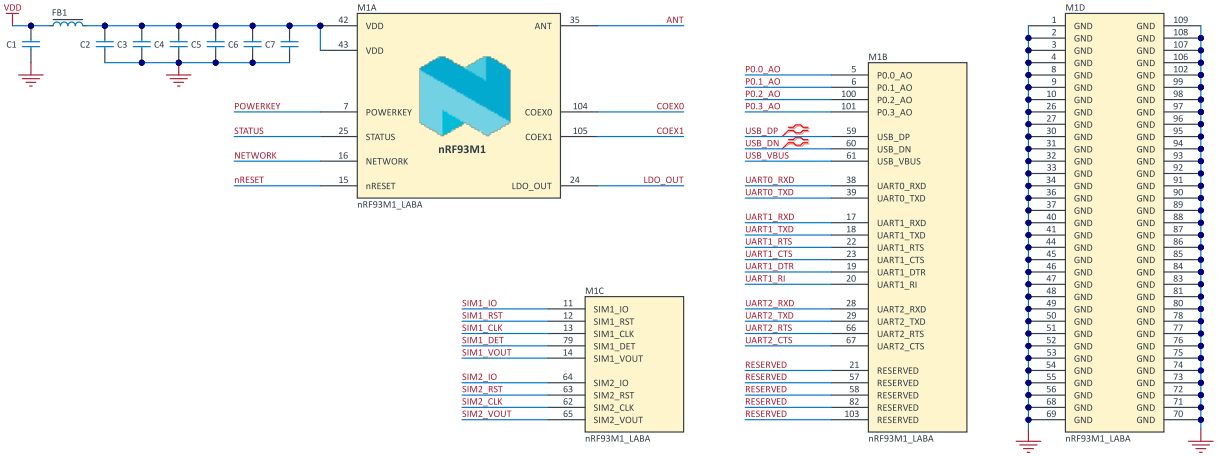

Figure 2: nRF93M1 application schematic drawing

The following table lists the recommended components for the nRF93M1 application schematic.

Designator	Recommended value	Description	Footprint
C1	4.7 µF	Capacitor, X5R, ±20%, 6.3 V	0402
C2, **C3**	100 µF	Capacitor, X5R, ±20%, 6.3 V	1206
C4	0.1 µF	Capacitor, X5R, ±10%, 10 V	0201
C5	100 pF	Capacitor, C0G, ±5%, 50 V	0201
C6	33 pF	Capacitor, C0G, ±5%, 50 V	0201
C7	8.2 pF	Capacitor, C0G, ±0.1 pF, 50 V	0402
FB1	22 Ω @ 100 MHz	Ferrite bead, 22 Ω @ 100 MHz, 6 A, 8 mΩ	0603

Table 2: Bill of materials for nRF93M1 application schematic

When selecting the components, take note of the following.

Capacitors (all types)

Higher temperature grade capacitors, such as the X6S series, are recommended if the product operates mainly in high temperature conditions (>65°C).

VDD capacitors

Lower voltage rating capacitors can be considered for products with a **VDD** voltage that is typically much lower than 4.5 V.

Smaller package size and capacitance value components can be used as long as the **VDD** voltage is 3.3 V under load. Current consumption peaks during TX.

The total capacitance in the **VDD** supply node affects current peaks (*Electromagnetic Interference (EMI)*) and voltage ripple at the **VDD** line. This can affect the end product's radiated performance.

Ferrite bead FB1

A smaller package size component can be used if the *EMI* performance and **VDD** voltage are at an acceptable level in the end product.

Use close to equal DC resistance and frequency characteristics as in the recommended component.

For recommended antenna matching component values and topology, see the *LTE* antenna datasheets.

3.2 Footprint, solder paste stencil, and reflow

The following figure and table show nRF93M1 mechanical drawing and dimensions.

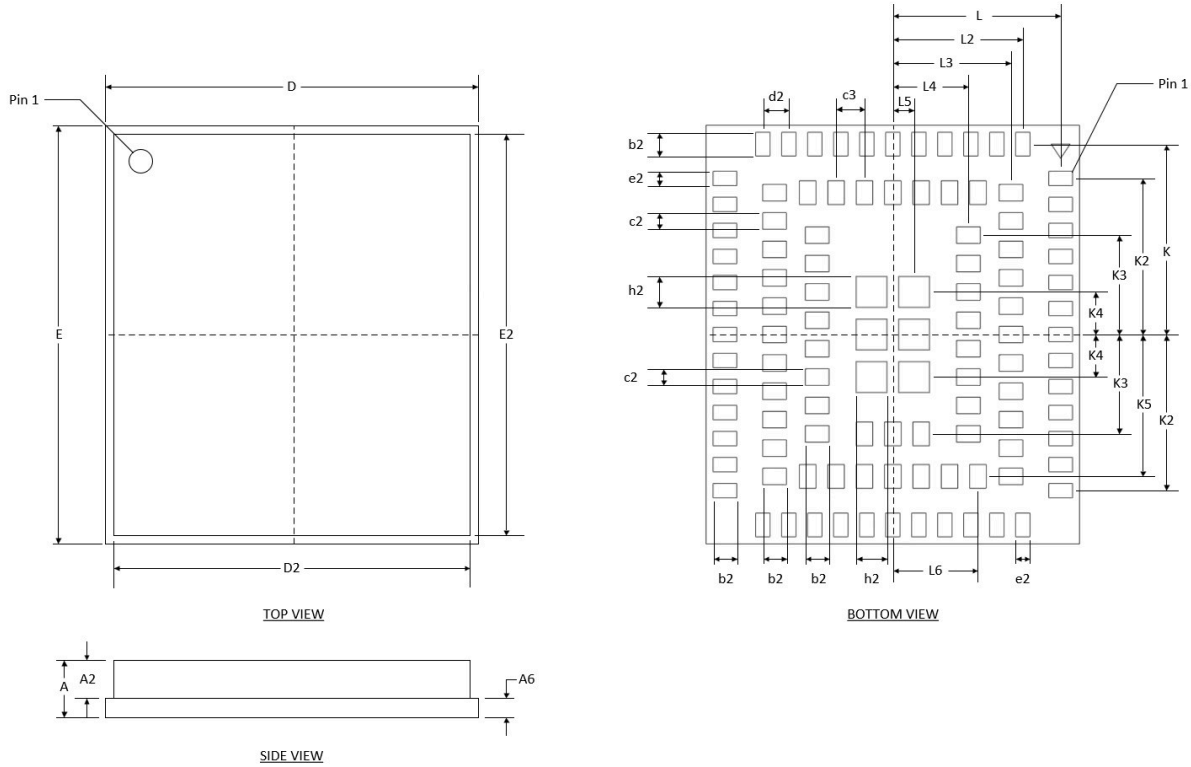

Figure 3: nRF93M1 mechanical drawing

	Min.	Nom.	Max.
A	2.2	2.4	2.6
A2		1.6	
A6		0.8	
b2		1	
c2		0.7	
c3		1.2	
D	15.65	15.8	15.95
D2		15.1	
d2		1.1	
E	17.55	17.7	17.85
E2		17	
e2		0.6	
h2		1.3	
K		8.05	
K2		6.6	
K3		4.2	
K4		1.8	
K5		6	
L		7.1	
L2		5.5	
L3		5	
L4		3.2	
L5		0.9	
L6		3.6	

Table 3: LGA mechanical specification (dimensions in mm)

Footprint recommendations

When designing the footprint, consider the following recommendations:

- Pad sizes should match the nominal size listed in the mechanical specification.
- For solder resist, either consult the *Printed Circuit Board (PCB)* vendor to get the correct size or use slightly larger openings, in the order of 50 µm. Having solder resist between pads reduces the risk of short circuits.

Solder paste stencil recommendations

Design the solder paste stencil in cooperation with your PCB assembly partner. Typically, the solder paste mask layer in the PCB manufacturing data is designed to have a one-to-one match with the exposed

copper area of footprint. The PCB assembly partner adjusts the solder paste mask layer based on their process and buys the stencil directly from their supplier.

If the solder paste stencil is designed without input from a PCB assembly partner, consider the following guidelines:

- Use a stencil thickness of about 100 µm. A thinner stencil improves solder paste release during printing but reduces the solder volume. A thicker stencil increases solder volume but increases the risk of short circuits.
- Use rounded corners in the stencil openings to improve the release of the solder paste from the stencil during the printing process.
- Adjust the solder volume on the pads to prevent short circuits and open joints during the assembly process.
    - Reduce the solder paster coverage for the first row to about 90% of the copper pad area of the footprint.
    - Reduce the solder paste coverage of the second and third row to about 80% of the copper pad area of the footprint.
    - Reduce the solder paste coverage of the largest six middle pads to approximately 70% of the copper pad area of the footprint.

Reflow conditions

For reflow profiling guidelines, refer to *IPC-7530, Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow and Wave), Figure 3-1 Thermal Profile Schematic*.

To avoid damage to the module caused by thermal stress, mount the module during the second-side production or to pass only once through the reflow oven.

Cleaning

The module uses a cupronickel shielding can with laser-marked identification on the surface. Use no-clean solder paste and a no-clean soldering process to avoid secondary cleaning after SMT assembly. Cleaning of the module after soldering is not recommended.

During soldering or any handling that may contact the module, do not wipe the shielding can, laser-marked area, label, QR code, or certification marking with organic solvents such as alcohol, isopropyl alcohol, acetone, trichloroethylene, or similar solvents. These solvents can cause oxidation or rusting of the shielding can and blurred or unreadable laser marking or QR codes.

Do not immerse the module in water, cleaning liquid, or chemical solvents. Do not apply high-pressure spray directly to the module, especially around shield gaps, RF areas, antenna pads, LGA pads, and component undersides.

If conformal coating, spraying, potting, or other surface treatment is required, ensure the material does not react with the module PCB, shielding can, markings, solder pads, or components, and does not flow into the module or cover antenna/RF-critical areas.

Do not use ultrasonic cleaning on the module; ultrasonic energy can damage crystals, oscillators, RF components, or other sensitive components inside the module. Do not use corrosive, halogen-containing, strong acid/alkaline, or unverified cleaning agents.

Solder voids

Solder voids are acceptable up to a certain level in the assembly process. Common rules for solder voids are the following:

- The maximum allowed void is 30% of the single pad surface area.

- If two voids are on the same pad, they must not touch each other as this can cause a crack-propagation path.
- Voids must not touch the pad edge.
- Avoid voids as these deteriorate thermal conduction performance. Higher ambient temperature increases this effect. Therefore, minimize voids to preserve nRF93M1's lifetime when the end product temperature is high.

3.3 GND

GND is the main electrical ground connection between nRF93M1 and the application board. It is also the main thermal dissipation path from nRF93M1 and the main mechanical connection.

The connection between **GND** and the application board must be electrically, thermally, and mechanically strong. It is recommended that the application board PCB's ground planes around nRF93M1 are as intact and as solid as possible. Use as many ground vias as possible between the top metal layer of the application board and the inner ground layers connected to nRF93M1's **GND** pins. Typically, metal filled vias provide the best thermal conductivity.

3.4 VDD

Power supply design is one of the main factors in achieving good RF performance, low current consumption, and reliable behavior of a product over its lifetime in various conditions. **VDD** (pins 42 and 43) is the main power supply input for nRF93M1.

VDD is connected to the nRF93M1-internal PMU that supplies the *System on Chip (SoC)* and the RF PA. The operational voltage of **VDD** ranges from 3.3 V to 4.5 V. A recommended supply voltage of 3.5 V should be able to output 1 A of current. For current consumption figures, see VDD current consumption on page 17.

To ensure operation as described in the nRF93M1 Preliminary Datasheet, it is important to prevent all voltage drops and ripples in **VDD** below 3.3 V during the operation of nRF93M1. Voltage drops due to high current draws are most likely to occur during *LTE* transmissions.

For *ESD* and *EMI* protection recommendations, see VDD on page 28 in ESD protection of nRF93M1 signals on page 28 and VDD on page 30 in EMI protection of nRF93M1 signals on page 30.

PCB layout design

When designing the PCB layout, consider the following recommendations for the **VDD** pin:

- Connect capacitors to the same ground plane as nRF93M1 using low impedance ground connections.
- Use wide enough tracks (DCR <0.1 Ω) for **VDD** routing to minimize voltage drops and unwanted power consumption coming from routing losses under high current conditions.
- Avoid supply routings close or adjacent to sensitive routings, such as RF.
- Use shielded PCB layers for routings whenever possible to minimize radiated noise.
- Use plenty of ground vias along supply routings to minimize unwanted voltage differences in the application PCB's metal layers.
- A series solder bridge is recommended in the **VDD** routing for current consumption measurements or other diagnostic purposes.

Note: Short low-impedance ground connections are mandatory for all supply capacitors.

3.4.1 VDD current consumption

During operation, nRF93M1 current consumption depends significantly on the *LTE* network, end product's antenna design, temperature, battery voltage, and the intensity of the LTE uplink data transmit. Although the typical current consumption of nRF93M1 can be very low, the power supply and system must be designed to meet the demands of the potential worst-case level of current consumption.

The worst level of current consumption depends, among other things, on the following:

- The temperature range for which the end product is certified.
- The cut-off voltage of the end product's power supply.
- The antenna impedance mismatch behavior when the end product is placed on a metal surface or covered by the user's hand.

Note: The most stringent target for current consumption in the design of the end product's supply is during extreme operating conditions. This means T_c > 55°C and antenna load that is not 50 Ω.

3.4.1.1 LTE Cat 1 bis current consumption for Power Class 3

The following table shows the average Power Class 3 current consumption of 3GPP *LTE* Cat 1 bis for a subframe (1 ms) during data transmission under both nominal and extreme operating conditions.

Average current consumption, Cat 1 bis, PC3, 5 MHz	Temp.	B8 (typ.)	B28 (typ.)	B3 (typ.)	B7 (typ.)	B40[1] (typ.)	Units
LTE subframe, P_{out} max, 3.3 V	–35°C	505	605	620	555	505	mA (50 Ω)
LTE subframe, P_{out} max, 3.8 V		500	595	625	560	515	mA (50 Ω)
LTE subframe, P_{out} max, 4.5 V		505	585	630	575	535	mA (50 Ω)
LTE subframe, P_{out} max, 3.3 V	25°C	520	580	615	555	510	mA (50 Ω)
LTE subframe, P_{out} max, 3.8 V		515	570	605	550	510	mA (50 Ω)
LTE subframe, P_{out} max, 4.5 V		510	545	585	540	515	mA (50 Ω)
LTE subframe, P_{out} max, 3.3 V	75°C	565	610	670	620	565	mA (50 Ω)
LTE subframe, P_{out} max, 3.8 V		550	590	650	610	565	mA (50 Ω)
LTE subframe, P_{out} max, 4.5 V		520	555	610	580	550	mA (50 Ω)

Table 4: LTE Cat 1 bis average current consumption during data transmission (Power Class 3)

The values in the tables represent typical average current consumption during uplink transmission. However, due to modulation, uplink transmission bursts contain current peaks that exceed the presented

[1] For TDD B40, the consumption includes TX only.

values. The duration of these peaks is in the range of a few microseconds and is related to system symbol duration. The following figures show examples of current consumption during a burst for Cat 1 bis data transmission.

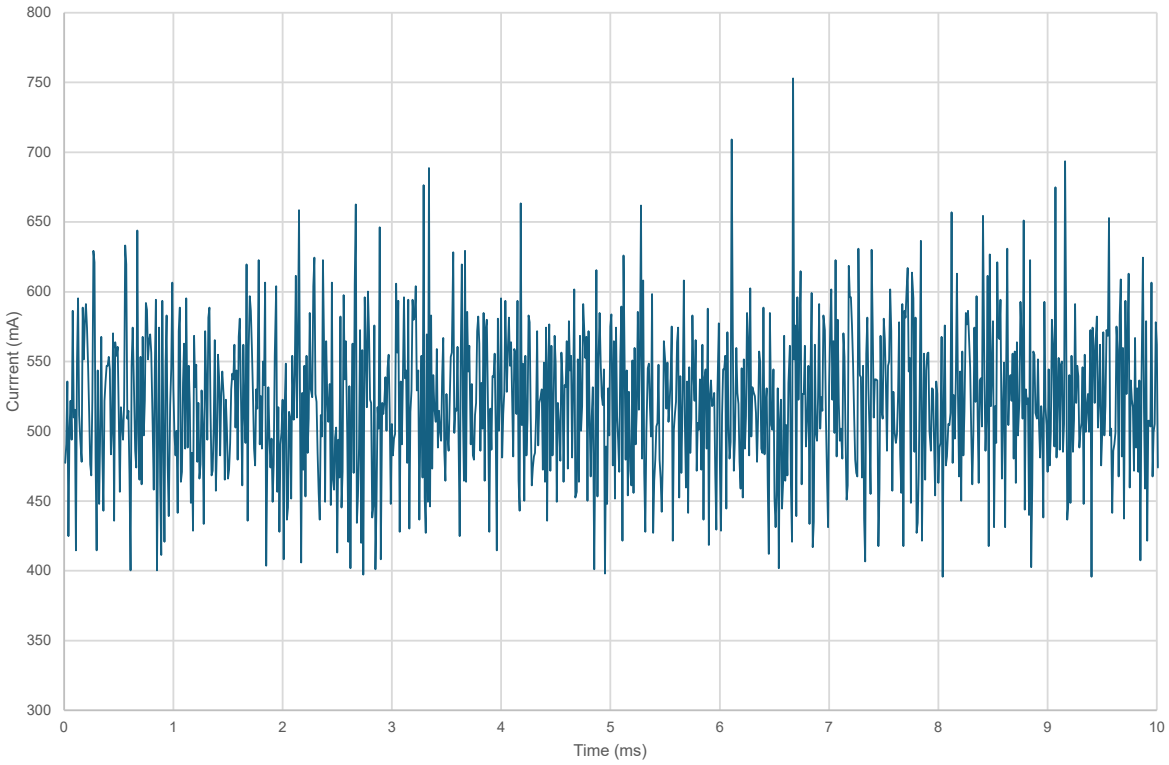

Figure 4: Example of current consumption during LTE Cat 1 bis data transmission (FDD)

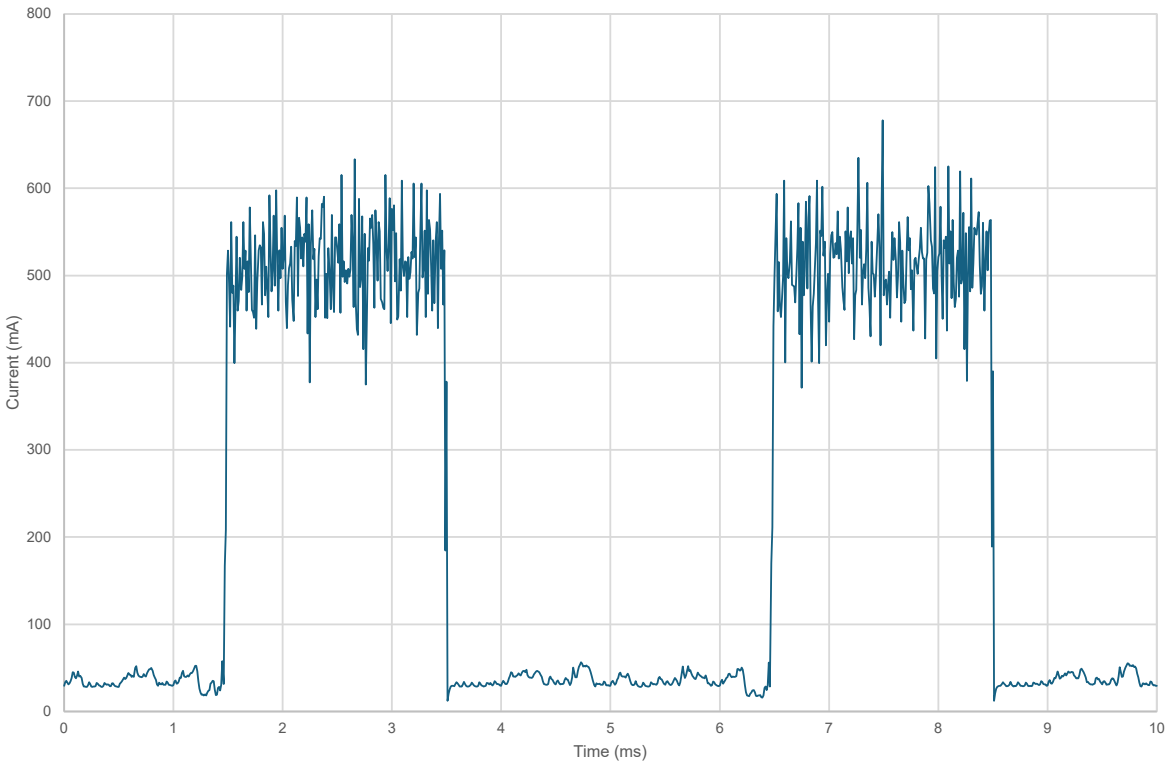

Figure 5: Example of current consumption during LTE Cat 1 bis data transmission (TDD)

3.5 LDO_OUT

LDO_OUT (pin 24) is a power output of the nRF93M1 module. The nominal voltage of the pin is 1.8 V and the maximum output current is 120 mA.

The **LDO_OUT** pin can be used to supply voltage for external pull-ups or reference levels. The **LDO_OUT** output is disabled during System OFF. Leave the pin floating if it is not used.

For *ESD* and *EMI* protection recommendations, see LDO_OUT on page 28 in ESD protection of nRF93M1 signals on page 28 and LDO_OUT on page 30 in EMI protection of nRF93M1 signals on page 30.

3.6 nRESET

nRESET (pin 15) is a dedicated nRF93M1 reset pin. A module reset is generated when the **nRESET** pin is pulled low for 300 ms. The pin can be connected to an external controller or mechanical switch that is controlled by the user.

When the **nRESET** pin is connected to an external controller, its voltage level should be taken into account in the design to avoid current leakage.

The **nRESET** pin has a 120 kΩ internal pull-up resistor connected to the nRF93M1 internal 1.15 V supply that is always on when the device is not in System DISABLED mode. The internal connection between the **nRESET** pin and the pull-up resistor is presented in Figure 6: nRESET pin on page 19. The connection consists of an internal series 10 kΩ resistor and a 0.1 µF parallel capacitor. Additional filtering components are not needed.

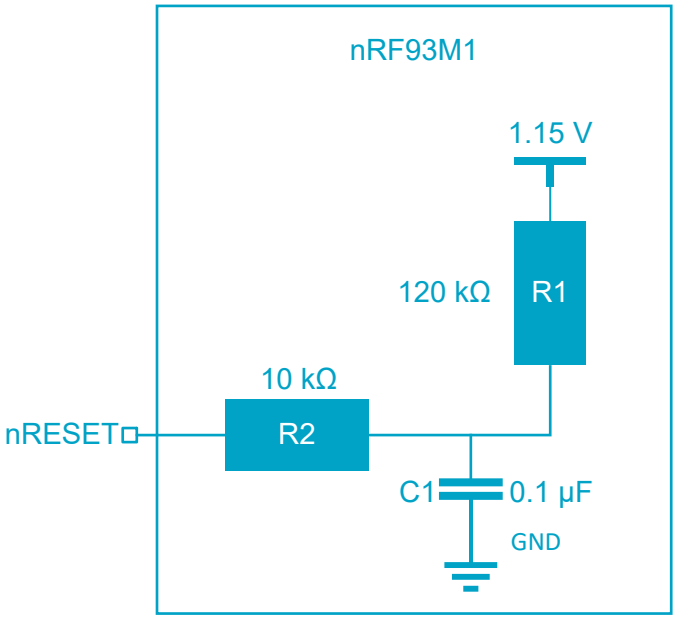

Figure 6: nRESET pin

To ensure that the reset is issued correctly, follow the pin reset timings and instructions in nRF93M1 Preliminary Datasheet.

Note:

- External pull-up is not allowed in the **nRESET** pin.
- External filtering components affect the minimum pulse length.

For *ESD* and *EMI* protection recommendations, see nRESET on page 28 in ESD protection of nRF93M1 signals on page 28 and nRESET on page 30 in EMI protection of nRF93M1 signals on page 30.

3.7 POWERKEY

POWERKEY (pin 7) is a dedicated nRF93M1 pin that makes the device enter and exit System DISABLE. A module reset is generated when the **POWERKEY** pin is pulled low. The pin can be connected to an external controller or mechanical switch that is controlled by the user.

The **POWERKEY** pin has a 180 kΩ internal always-on pull-up resistor that is connected to the nRF93M1 internal supply. The voltage level of the pull-up is typically 1.4 to 2.4 V and depends on the **VDD** voltage level. The internal connection between the **POWERKEY** pin and the pull-up resistor is presented in Figure 7: POWERKEY pin on page 20. The connection consists of an internal series 10 kΩ resistor and a 0.1 µF parallel capacitor. Additional filtering components are not needed.

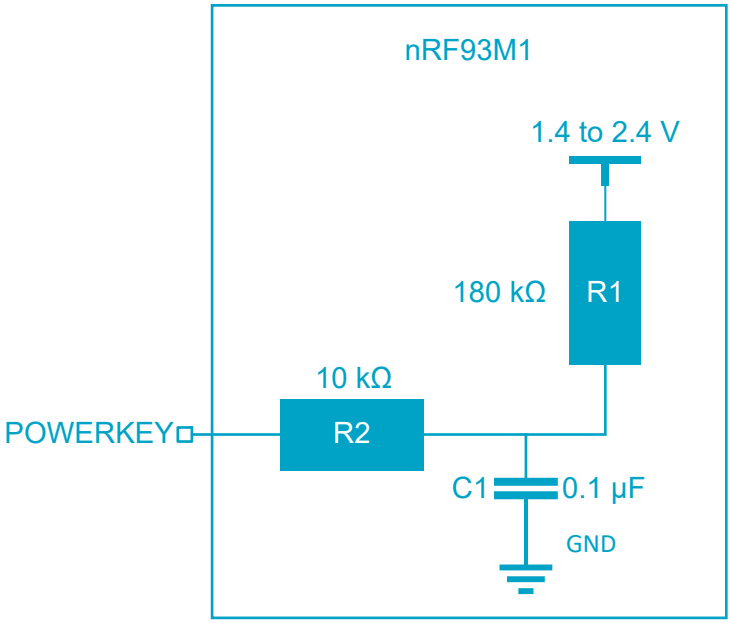

Figure 7: POWERKEY pin

To ensure that the reset is issued correctly, follow the pin reset timings and instructions in nRF93M1 Preliminary Datasheet.

For *ESD* and *EMI* protection recommendations, see POWERKEY on page 29 in ESD protection of nRF93M1 signals on page 28 and POWERKEY on page 31 in EMI protection of nRF93M1 signals on page 30.

3.8 STATUS

STATUS (pin 25) indicates the nRF93M1 operational status. The pin is high when the module is powered, initialized and running normally.

When **STATUS** is low, do not drive any non-wake-up pin high to avoid current leakage.

The **STATUS** pin is connected to the internal 1.8 V voltage domain. Leave the pin floating if not in use.

For more information, see nRF93M1 Preliminary Datasheet.

For *ESD* and *EMI* protection recommendations, see STATUS on page 29 in ESD protection of nRF93M1 signals on page 28 and STATUS on page 31 in EMI protection of nRF93M1 signals on page 30.

3.9 NETWORK

NETWORK (pin 16) indicates the nRF93M1 network status. The pin pulses at different duty cycles to indicate the connection state.

The **NETWORK** pin is connected to the internal 1.8 V voltage domain. Leave the pin floating if not in use.

For more information, see nRF93M1 Preliminary Datasheet.

For *ESD* and *EMI* protection recommendations, see NETWORK on page 29 in ESD protection of nRF93M1 signals on page 28 and NETWORK on page 31 in EMI protection of nRF93M1 signals on page 30.

3.10 UICC

nRF93M1 has two *UICC* interfaces: SIM1 and SIM2. The UICC interface is used to communicate with a *Universal Subscriber Identity Module (USIM)* or *Embedded SIM (eSIM)*. The UICC interface is commonly known as the *Subscriber Identity Module (SIM)* card interface.

SIM1 consists of **SIM1_IO** (pin 11), **SIM1_RST** (pin 12), **SIM1_CLK** (pin 13), **SIM1_DET** (pin 79), and **SIM1_VOUT** (pin 14).

SIM2 consists of **SIM2_IO** (pin 64), **SIM2_RST** (pin 63), **SIM2_CLK** (pin 62), and **SIM2_VOUT** (pin 65).

nRF93M1 supports UICC Class C interface with 1.8 V nominal voltage and UICC Class B with 3.0 V nominal voltage. If two external SIMs are used, both must use the same class and voltage. nRF93M1 automatically detects the UICC class.

The LTE modem controls the following physical interfaces towards the UICC and implements the transport protocol over the ISO/IEC 7816-3 interface.

- **SIM_VOUT** – power supply, 1.8 V or 3.0 V, auto-selected depending on the SIM card
- **SIM_CLK** – clock signal, LTE modem driven
- **SIM_RST** – reset signal, LTE modem driven
- **SIM_IO** – input/output serial data, bi-directional
- **SIM_DET** – card detection, only available on SIM1

SIM1_DET detects high polarity. Use a normally closed SIM holder for applications where SIM1 stays connected most of the time. This eliminates extra current consumption.

nRF93M1 has only one SIM supply. **SIM1_VOUT** and **SIM2_VOUT** are on the same net inside the module.

For *ESD* and *EMI* protection recommendations, see SIM / UICC on page 28 in ESD protection of nRF93M1 signals on page 28 and SIM / UICC on page 30 in EMI protection of nRF93M1 signals on page 30.

3.11 USB

The nRF93M1 module supports the USB 2.0 interface and complies with the USB 2.0 specification. It supports Full-Speed (12 Mbps) and High-Speed (480 Mbps) operation.

nRF93M1 supports only USB device/peripheral mode. You can connect the USB interface on nRF93M1 to a USB connector or to a USB interface on a host *MCU*.

The USB peripheral consists of the **USB_DP** (pin 59), **USB_DM** (pin 60), and **USB_VBUS** (pin 61) pins. If **USB_VBUS** is applied during System OFF, nRF93M1 wakes up. Leave these pins floating when they are not in use.

PCB layout design

When designing the PCB layout, consider the following recommendations for the USB pins:

- Maintain a differential impedance of 90 Ω for the **USB_DP** and **USB_DM** routing and treat the surrounding area with a ground.
- To prevent USB signals from generating *EMI* interference, place a common-mode inductor at the USB connector. See USB on page 31 in EMI protection of nRF93M1 signals on page 30 for more information.
- Keep USB traces away from crystal oscillators, oscillators, magnetic devices, RF signals, and strong signal areas.
- If the USB interface of nRF93M1 is exposed to external *ESD* events, add ESD protection. See USB on page 29 in ESD protection of nRF93M1 signals on page 28 for more information.

3.12 P0.0_AO–P0.3_AO

nRF93M1 provides pins for wake-up and for controlling external RF devices.

For *ESD* and *EMI* protection recommendations, see P0.0_AO-P0.3_AO on page 28 in ESD protection of nRF93M1 signals on page 28 and P0.0_AO-P0.3_AO on page 30 in EMI protection of nRF93M1 signals on page 30.

P0.0_AO

The **P0.0_AO** (pin 5) pin is a dedicated wake-up pin for the nRF93M1. It is connected to the internal always-on 1.8 V voltage domain.

Leave the pin floating if it is not used.

P0.1_AO-P0.3_AO

The pins **P0.1_AO** (pin 6), **P0.2_AO** (pin 100), and **P0.3_AO** (pin 101) are dedicated to controlling external RF devices such as antenna tuners. They are connected to the internal 1.8 V voltage domain.

Leave the pins floating if they are not used. It is not recommended to use external pull-down resistors.

The pins can be configured to high or low states based on the active RF band. For more information, see the `%RFC` command in the nRF93M1 AT Commands reference guide.

3.13 COEX interface

The nRF93M1 has a two-pin COEX interface (pins 104 and 105). It is dedicated to RF control and interference avoidance towards a companion radio device, such as an external positioning device or *Bluetooth*® Low Energy device.

The COEX interface is flexible and can be configured using AT commands. See the nRF93M1 AT Commands reference guide for more information.

The COEX interface is powered from the internal 1.8 V voltage domain. During System OFF, COEX pins are floating. Therefore, it is mandatory to use external pull-down resistors in the size range of 100 kΩ in the COEX interface. If COEX pins are not in use, leave them floating.

For *ESD* and *EMI* protection recommendations, see COEX on page 28 in ESD protection of nRF93M1 signals on page 28 and COEX on page 30 in EMI protection of nRF93M1 signals on page 30.

3.14 UART interface

The nRF93M1 has three *Universal Asynchronous Receiver/Transmitter (UART)* interfaces: UART0, UART1, and UART2.

The UART interface is powered from the internal 1.8 V voltage domain. This means they turn off during nRF93M1 System OFF mode. UART1 supports wake-up functionality. Leave unused UART pins floating.

The following tables show the UART pins, and where they are connected to on the host *MCU*.

Pin number	Pin name – UART0	To host MCU's
38	**UART0_RXD**	**TXD**
39	**UART0_TXD**	**RXD**

Table 5: UART0 pins

Pin number	Pin name – UART1	To host MCU's
17	**UART1_RXD**	**TXD**
18	**UART1_TXD**	**RXD**
22	**UART1_RTS**	**CTS**
23	**UART1_CTS**	**RTS**
19	**UART1_DTR**	**DTR**
20	**UART1_RI**	**RI**

Table 6: UART1 pins

Pin number	Pin name – UART2	To host MCU's
28	**UART2_RXD**	**TXD**
29	**UART2_TXD**	**RXD**
66	**UART2_RTS**	**CTS**
67	**UART2_CTS**	**RTS**

Table 7: UART2 pins

For *ESD* and *EMI* protection recommendations, see UART on page 29 in ESD protection of nRF93M1 signals on page 28 and UART on page 31 in EMI protection of nRF93M1 signals on page 30.

3.15 ANT

ANT (pin 35) is a 50 Ω single-end interface for the *LTE* antenna. To ensure good performance, antenna impedance and the characteristic impedance of the transmission line connecting the antenna to the **ANT** pin must be 50 Ω. Impedance mismatch leads to performance deterioration.

Keep the length of the transmission line from the antenna to the **ANT** pin as short as possible. This reduces signal losses in transmission and reception for nRF93M1 which improves power consumption and network coverage. A maximum of 0.5 dB loss in the transmission line is acceptable.

ESD protection is required if the application design includes ESD events that might occur in the antenna port. See the component datasheet for device requirements. See nRF93M1 Preliminary Datasheet for nRF93M1 ESD ratings. See ANT on page 29 in ESD protection of nRF93M1 signals on page 28 for design recommendations.

For *EMI* protection recommendations, see ANT on page 31 in EMI protection of nRF93M1 signals on page 30.

The **ANT** pin is DC grounded. A matching network of a minimum of three components is typically needed close to the antenna. The component values and matching topology depend on the antenna application and antenna path impedance and need to be optimized individually for each design.

PCB layout design

When designing the PCB layout, consider the following recommendations for the **ANT** pin:

- To ensure good radiated performance, begin the design by locating the LTE antenna on the PCB.
- Ensure preliminary antenna performance on a chosen PCB location, for example, by simulation.
- When multiple antennas, for example, LTE, *Global Navigation Satellite System (GNSS)*, and Bluetooth Low Energy are present, minimize antenna crosstalk.
- Antenna transmission line impedance should be 50 Ω. Take this into account when selecting the PCB stack-up.
- Avoid excessive capacitance in routing by opening ground layers under component pads. For example, if the routing is on the top PCB layer, open the ground plane under the **ANT** pad on the next metal layer.
- When opening ground planes, avoid exposing noisy routings under the **ANT** pad.
- Favor routing in shielded PCB layers to minimize radiated noise coupling to the ANT line.
- Avoid long routing because it causes excessive insertion loss which deteriorates RF performance.
- Ensure a continuous reference ground plane above, below, or both of the ANT routing.
- Consider adding a test connector to the antenna path for production test and diagnostic purposes. Ensure that the test connector or solution does not deteriorate the impedance of the transmission line.

3.16 Reserved

Pins 21, 57, 58, 82, and 103 are reserved for Nordic's internal diagnostic purposes. It is recommended to connect the **RESERVED** pins to the application board mechanically and thermally, but to keep them electrically unconnected.

4 Hardware design

The design of an end product is often driven by a small form factor and attractive appearance. However, to achieve a product with solid performance, several design factors must be considered.

Some design factors conflict with the small form factor target. Typically, this means a compromise in the design that can affect the performance or appearance of the end product.

When a preliminary schematic of the device is ready, designing the PCB can begin. Layout design is typically iterative and involves trade-offs. The first hardware design rarely ends up being the mass-produced version. To minimize the number of hardware design rounds, cost, and time, the selected essential design factors that have a major impact on the end product's RF performance are discussed here.

4.1 Component placement

It is recommended to categorize and prioritize connections between nRF93M1 and application components based on their criticality.

The main principle in placing nRF93M1 is to optimize the routing of the highest priority connections. Additionally, it is important to ensure good thermal and mechanical contact with the application board and to avoid placing nRF93M1 near noisy components like buck regulators or high-frequency signals.

RF routings are the most critical for nRF93M1's performance due to the mandatory impedance control and their noticeable impact on user experience. Ensuring sufficient power supply routings are also important for optimal operation. In addition, the *SIM* interface is sensitive and should be given priority in the layout.

It is recommended to categorize application components according to which ones can be adjacent to one another on the PCB. For example, sensitive antennas should not be placed next to noisy buck regulators or LEDs. Two antennas, such as Bluetooth Low Energy and *LTE*, should never be adjacent to each other due to the risk of mutual load effect between two nearby radiators. This interference can significantly deteriorate antenna efficiency and radiation pattern, severely impacting the overall performance of the end product.

Some components, such as the LTE antenna and SIM holder, should be placed close to nRF93M1 to minimize the negative effects of long PCB routing, but they should not be near each other. These components should not be too far from nRF93M1, but their mutual distance should be maximized. If possible, it is recommended to place these components on the opposite sides of the PCB.

Based on connections and component categorization, you can begin the layout and component placement mockup. Start the layout work from the most critical routings. For a best practice design, each signal layer should have an adjacent metal layer, that is, ground plane, which is dedicated to signal return currents. This metal layer also serves as the main path for thermal dissipation and power relief for nRF93M1 and other active components on the application board.

A small form factor PCB sets constraints for component placement, especially for the antenna and its ground layer. Optimal placement for antennas is important and helps guarantee radiated performance and good user experience for the end product. Therefore, it is recommended to use EM simulation tools to estimate the impact of different antenna locations and grounding on the PCB. Antenna design and simulation services are provided by various design houses globally.

Antenna vendors often provide design and measurement services, but these are typically for their own products. If the end product includes antennas from multiple vendors, it is important to ensure that all antennas are verified to perform as expected when used together in the end product.

4.2 OTA performance

If a small form factor device integrates antennas with noticeable performance requirements, such as *LTE*, the antenna-related design should be prioritized.

The key requirement in antenna design is that all antennas fulfill their performance targets in the actual use cases of the end product. The efficiency target for LTE antennas should be a minimum of 50%.

Troubleshooting

This section describes typical performance related issues in the end product's antenna design and ways to reduce them.

Harmonic performance worse than expected

In several customer studies where poor radiated harmonic performance was observed, the root cause was traced to a non-linear active component that was located close to the LTE antenna and increased the harmonic level. In this scenario, the nRF93M1 TX signal couples into a nearby component where it becomes distorted, generates harmonics, and increases the overall harmonic levels.

To prevent poor radiated harmonic performance, the following scenarios should be avoided:

- TX signal coupling to another antenna, active device, or component on the board. Performance might be further degraded if another device is powered off as it can behave more non-linearly.
- nRF93M1 antenna trace is not 50 Ω.
- LTE antenna and its matching is not 50 Ω.

The placement of the antenna on the PCB and ground plane prevents from achieving good enough antenna radiation performance.

Follow the antenna vendors' recommendations for placing the antenna on the PCB and ground plane.

Verify the antenna radiation pattern and efficiency in an anechoic chamber to match the datasheet.

RF path routing loss between antenna and nRF93M1 is too high.

Verify 50 Ω impedance-controlled routing between the antenna and nRF93M1.

Target is less than 0.5 dB for resistive loss between the antenna and nRF93M1.

Mechanics, casing, battery, or wires deteriorate antenna performance.

Co-design the mechanics to match the PCB and antenna design.

Sharing a small PCB between several antennas causes mutual loading between the antennas.

Verify that the antennas do not cause mutual loading, for example, with passive antenna measurements in an anechoic chamber.

Terminating an unused antenna can have a noticeable impact on the mutual loading effect between the antennas.

Active components on the PCB cause wideband noise coupling to the antennas.

Verify that during reception, active components on the PCB do not radiate noise to the antennas. For example, buck regulators and LEDs are typical sources of radiating wideband noise. The RSSI scan testing method can be used.

The orientation of the end product in a typical use case is less than optimal for the antenna radiation pattern.

Consider in the design phase what the orientation of the end product is going to be in a typical use case.

Nearby objects deteriorate antenna performance.

Instruct the end user to use the device in the manner it is designed for. For example, inform the user not to expect the best possible radio performance when the device is used inside a building, on a metal surface, or on their body.

4.3 nRF93M1 module

The main principle in placing the nRF93M1 module on the application board is to optimize the highest priority routings as described in Component placement on page 25.

It is also important to ensure good thermal and mechanical contact between the nRF93M1 module and the application board. Do not place nRF93M1 near noisy components, such as buck regulators or LEDs.

4.4 PCB stack-up

Choosing the PCB stack-up should be aligned with the end product's PCB requirements.

For nRF93M1, the following targets should be considered:

- For a best practice design, each signal layer should have an adjacent metal layer, that is, ground plane, which is dedicated to signal return currents.
- Consider the need for 50 Ω RF routings. Sometimes, to achieve 50 Ω routing requires opening the adjacent metal layer, which increases the risk of exposing RF routing to noisy routings.
- Avoid crossing 50 Ω RF routings on the application board. If it cannot be avoided, ensure that their ground planes remain continuous.
- Avoid using through vias in RF routings if they cause a parallel stub to the routing or are not 50 Ω.
- Consider good thermal design and aim to use metal filled vias due to their better thermal conductivity, especially when they are near nRF93M1.

4.5 ESD protection

ESD protection routes electrostatic discharge energy to ground and the relevant supply domain before it can damage nRF93M1 or cause latent defects.

The basic idea for ESD protection is to provide a low-impedance path between any IO signal pin and both **GND** and its reference supply voltage domain whenever the voltage level at the protected IO signal pin goes beyond its native voltage range during an ESD event, as defined in the product specification. An ESD event can lead to immediate catastrophic failure or latent defects in the nRF93M1 module.

An ESD event is very likely to happen in any end product where conductive surfaces are exposed to the surrounding environment (for example, connectors). Protect those interfaces to prevent ESD sparks from reaching the internal electronics. Also, long cables are susceptible to ESD events due to their antenna-like properties. High magnetic or electric fields might induce unwanted currents and voltages in the cable conductors.

Place ESD protection as close to the entry point as possible (for example, as close to the connector as possible) to prevent the ESD charge from entering other parts of the *PCB*. Design ESD protection in such a way that parasitic inductances are minimized. Parasitic inductances on the **GND** reference plane play a crucial role in successful ESD protection design and are often overlooked.

IO signal protection is typically done with *Transient Voltage Suppressor (TVS)* diodes, but sometimes an additional low-pass circuit might also be required. The designer must consider how much capacitance each IO signal can handle so that signal rise and fall times comply with the intended operation. As mentioned above, it is crucial to arrange a low-impedance path to both **GND** and the IO signal supply rail

during an ESD event. For example, a 1.8 V IO signal should ideally have a clamp to both **GND** and the 1.8 V voltage domain to protect the IO domain efficiently against both polarities of the ESD event.

Supply nets (for example, **VDD** and **GND**) are as susceptible to ESD events as IO signals but, due to the intrinsic nature of those nets, are usually well protected by decoupling capacitors. Capacitors dampen high-voltage events and act as a low-impedance path during the fast rise and fall periods of an ESD event, which in most cases provides enough protection. However, some supply nets (for example, the *SIM* interface) do not include much capacitance and should incorporate ESD protection for the supply net if exposed to ESD events.

In some cases, it might also be necessary to protect the main supply lines with additional protection mechanisms like spark gaps or ESD diodes, but that depends highly on the end product ESD protection requirements. When designing ESD protection for supply nets, select protection devices carefully because some ESD protection diodes might leak current when reverse biased and cause unwanted current consumption in low-power *Internet of Things (IoT)* devices.

4.5.1 ESD protection of nRF93M1 signals

This section summarizes *ESD* protection recommendations for each nRF93M1 interface.

VDD

The reference design for nRF93M1 includes high capacitive decoupling from the **VDD** pin to **GND** and thus typically does not require additional ESD protection measures. However, if the customer design exposes the **VDD** pin to external ESD events, consider additional ESD protection measures in the product *PCB* design. Follow the general instructions for supply protection in ESD protection on page 27.

LDO_OUT

The **LDO_OUT** pin has quite low capacitive decoupling to **GND**, which does not provide good ESD protection. If the customer design exposes the **LDO_OUT** pin to external ESD events, consider additional ESD protection measures in the product PCB design.

SIM / UICC

The *SIM* interface requires ESD protection if the SIM interface is exposed to external ESD events (for example, a replaceable SIM card). Use ESD protection devices that are designed for the SIM interface and that also protect the **SIM_VOUT** voltage domain.

P0.0_AO-P0.3_AO

ESD protection is required for pins that are exposed to external ESD events. Follow the general instructions for IO signal protection in ESD protection on page 27.

COEX

ESD protection is required for pins that are exposed to external ESD events. Follow the general instructions for IO signal protection in ESD protection on page 27.

nRESET

ESD protection is required if the **nRESET** pin is exposed to external ESD events. Follow the general instructions for IO signal protection in ESD protection on page 27.

POWERKEY

ESD protection is required if the **POWERKEY** pin is exposed to external ESD events. Follow the general instructions for IO signal protection in ESD protection on page 27.

STATUS

ESD protection is required if the **STATUS** pin is exposed to external ESD events. Follow the general instructions for IO signal protection in ESD protection on page 27.

NETWORK

ESD protection is required if the **NETWORK** pin is exposed to external ESD events. Follow the general instructions for IO signal protection in ESD protection on page 27.

UART

ESD protection is required if *UART* pins are exposed to external ESD events. Follow the general instructions for IO signal protection in ESD protection on page 27.

USB

The USB interface requires ESD protection if the USB interface is exposed to external ESD events (for example, a USB connector). Use ESD protection devices that are designed for the USB interface and that also protect the **USB_VBUS** voltage domain.

ANT

The **ANT** pin requires ESD protection if it is exposed to external ESD events (for example, a replaceable antenna). Implement RF signal protection with ESD diodes that are designed for high-frequency usage. The protection device must have bidirectional configuration with equal breakdown voltages in both directions and ultra-low capacitive loading (<< 1 pF) so that the impact on RF signal line impedances is negligible during normal operation.

4.6 EMI protection

EMI protection uses filter circuits to reduce noise generated by internal circuitry and to protect nRF93M1 IO signals from external noise.

The basic idea for EMI protection is to use filter circuits that dampen noise generated by internal circuitry or protect the nRF93M1 module IO signals from external noise. Noise generated by the nRF93M1 internal circuitry can radiate out and cause, for example, *Electromagnetic Compatibility (EMC)* test failures on regulatory tests or radio receiver performance issues. In contrast, external noise injected into nRF93M1 signal pins can cause unwanted behavior in nRF93M1 operation (for example, resets or unwanted IO pin triggering) or even radiated emissions due to non-linear circuit elements (for example, internal *ESD* protection diodes).

Nordic Semiconductor recommends adding EMI protection on all supply lines that include *Switched-Mode Power Supply (SMPS)* circuits on the customer *PCB*. SMPS circuits typically generate wideband noise that can reach 1 GHz or higher and cause the problems mentioned above. The recommended EMI protection for supply lines is a Pi-type filter (capacitor - ferrite - capacitor) positioned as close to the noise source as possible.

IO signal EMI protection can be constructed with a simple RC or LC low-pass filter and, in some cases, with a plain capacitor. High-frequency interfaces (for example, USB) usually require more dedicated protection devices, which are commonly available from several component vendors. The protection design depends

highly on the use case, and it is not possible to provide instructions that cover all use cases. General EMI protection notes for each pin on the nRF93M1 module are presented in EMI protection of nRF93M1 signals on page 30.

Additionally, other signals on the customer end product that are not directly related to nRF93M1 might need EMI protection. During TX transmissions, the nRF93M1 module radiates at relatively high power levels, which might couple to poorly RF-shielded areas on the customer board that can act as receiving antennas. For example, flex PCBs or components that have large internal coils (for example, speakers or transducers) have such properties. When TX power couples into these circuits, non-linear elements (for example, internal ESD protection diodes in *Integrated Circuit (IC)* components) might generate unwanted harmonic emissions that can cause failures in regulatory EMC tests. Analyze whether these coupling paths exist on the customer end product and protect them with relevant filters.

4.6.1 EMI protection of nRF93M1 signals

This section summarizes *EMI* protection recommendations for each nRF93M1 interface.

VDD

Add a Pi-type low-pass filter (capacitor - ferrite - capacitor) to filter out noise generated by the internal *SMPS*. Ideally, the filter should cover the frequency range from <1 MHz up to 2 GHz.

LDO_OUT

Generally, no EMI protection is required due to low output noise content. The internal output capacitance keeps impedance low at high frequencies and should not cause emissions in the module's internal *ESD* protection diodes.

SIM / UICC

Generally, no EMI protection is required. However, if the *SIM* signals in the end product design are routed somewhere (for example, on a flex *PCB*) that might lead to high-power RF signal coupling into the interface signal traces, additional filtering might be required to prevent unwanted pin toggling or harmonic emissions in the internal ESD protection diodes.

P0.0_AO-P0.3_AO

Generally, no EMI protection is required. However, if the signals in the end product design are routed somewhere (for example, on a flex PCB) that might lead to high-power RF signal coupling into the signal traces, additional filtering might be required to prevent unwanted pin toggling or harmonic emissions in the internal ESD protection diodes.

COEX

Generally, no EMI protection is required. However, if the COEX signals in the end product design are routed somewhere (for example, on a flex PCB) that might lead to high-power RF signal coupling into the signal traces, additional filtering might be required to prevent unwanted pin toggling or harmonic emissions in the internal ESD protection diodes.

nRESET

Nordic Semiconductor recommends adding a decoupling capacitor near the **nRESET** pin to prevent unwanted reset signal generation.

POWERKEY

Generally, no EMI protection is required. However, if the **POWERKEY** pin is routed somewhere in the end product design (for example, on a flex PCB) that might lead to high-power RF signal coupling into the signal trace, additional filtering might be required to prevent unwanted pin toggling or harmonic emissions in the internal ESD protection diodes.

STATUS

Generally, no EMI protection is required. However, if the **STATUS** pin is routed somewhere in the end product design (for example, on a flex PCB) that might lead to high-power RF signal coupling into the signal trace, additional filtering might be required to prevent harmonic emissions in the internal ESD protection diodes.

NETWORK

Generally, no EMI protection is required. However, if the **NETWORK** pin is routed somewhere in the end product design (for example, on a flex PCB) that might lead to high-power RF signal coupling into the signal trace, additional filtering might be required to prevent harmonic emissions in the internal ESD protection diodes.

UART

Generally, no EMI protection is required. However, if the *UART* signals in the end product design are routed somewhere (for example, on a flex PCB) that might lead to high-power RF signal coupling into the signal traces, additional filtering might be required to prevent unwanted pin toggling or harmonic emissions in the internal ESD protection diodes.

USB

If nRF93M1 interfaces with an external *MCU* or processor on the same PCB, additional EMI protection is generally not required. If the nRF93M1 USB interface is connected to a USB connector, Nordic Semiconductor recommends adding a common-mode filter designed for the USB signal interface close to the USB connector to prevent radiated emissions from the USB signal lines. Additionally, filter the USB power lines (the **USB_VBUS** pin and the **GND** pin), for example with a Pi-type filter, for the same reason.

ANT

Generally, no EMI protection is required if the antenna interface (RF trace and antenna) is correctly designed. If you add EMI protection, ensure that the design follows generic RF design rules (for example, impedance matching).

5 R&D and QA verification

This section describes measurements on power consumption, *UICC* interface, and RF to verify performance and quality of the product.

5.1 Check supply voltages

The expected values of the voltage levels on the **VDD** and **LDO_OUT** pins are shown in the following table.

Parameter	Min.	Typ.	Max.	Description
VDD voltage	3.3 V		4.5 V	Main power supply input voltage (external supply)
LDO_OUT		1.8 V		Module internal power supply for UART and power output

*Table 8: Voltage levels of **VDD** and **LDO_OUT***

Note: **LDO_OUT** is not active during sleep modes.

5.2 Testing RF performance

The RF performance of nRF93M1 is designed to meet the 3GPP *TS 36.101* specification. RF performance can be tested with a cellular tester that supports RF measurements specified in the 3GPP specification, such as Rohde & Schwartz CMW100 or CMW500.

Radiated performance should also be verified. This testing requires an anechoic RF chamber and is typically conducted by a test house that provides this service. The following figure shows an example setup for a signaling mode RF performance test.

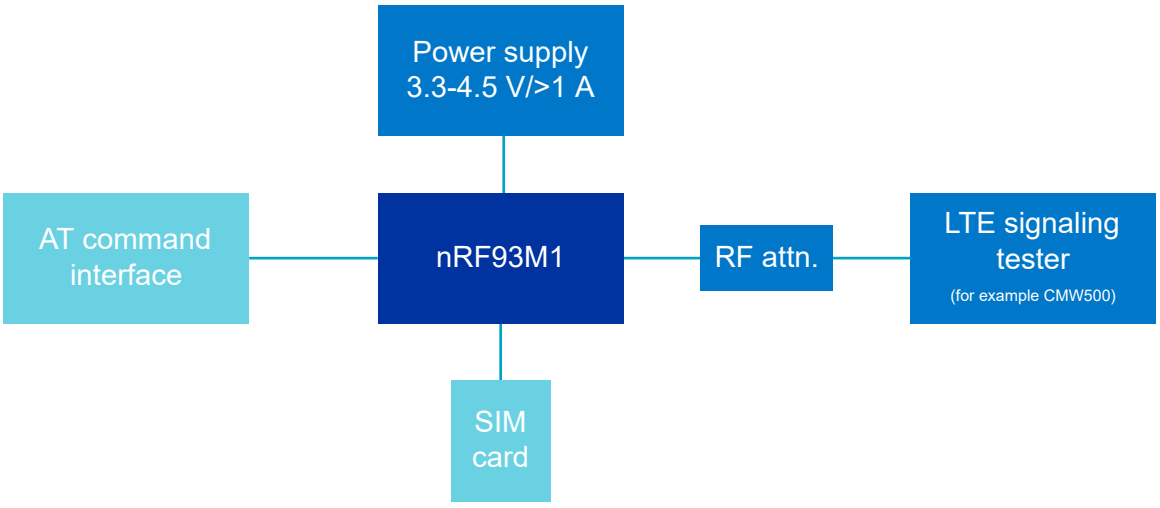

Figure 8: Signaling mode RF test setup

5.2.1 RF conducted performance test

RF conducted performance test is recommended to be performed in the R&D phase to verify the RF performance of the end product. A verified conducted test provides a solid background for entering radiated RF tests.

The tests should be performed with a 50 Ω test connector or soldered cable.

5.2.1.1 Signaling mode

In the signaling mode, a connection is established towards the tester, and nRF93M1 is controlled over an RF interface in the same way as in a real cellular network.

Mode	Test item	3GPP test ID	Band/ channel	Temp./ voltage	Signaling parameters	Expected result	Comment
Cat 1 bis TX	Maximum output power	6.2.2EB	ALL/ LMH	TYP/ TYP	5 MHz, QPSK (RMC)	23 dBm	P_{max}, 23 dBm, ±2 dB (5 MHz, 1 RB)
	Frequency error	6.5.1EB	ALL/ MID	TYP/ TYP		<±0.1 ppm	
	PUSCH EVM (RMS)		ALL/ LMH	TYP/ TYP		<7%	P_{max}, 3GPP limit <17.5%
	Adjacent channel leakage power ratio	6.6.2.3EB				<-35 dBc	P_{max}, (5 MHz, 25 RB) E-UTRA ±1
	Spurious emission (9 kHz to 12.75 GHz)	6.6.3.1	ALL/ MID	TYP/ TYP		<-33 dBm/ 1 MHz	P_{max}, Harmonics, spurious, noise
Cat 1 bis RX	Reference sensitivity level	7.3EB	All/ LMH			<-99 dBm	P_{max},5 MHz, 25 RB

Table 9: RF performance tests for conducted signalling mode

Measuring receiver sensitivity for all channels is time-consuming but reveals any spurious or noise coupled to the nRF93M1 antenna port.

6 Production test

The test flow described in this section provides an example of the production test process for a product based on nRF93M1. nRF93M1 is fully tested and calibrated in the Nordic Semiconductor production line. The main focus of a product-level production test is checking for assembly related errors.

Production tests are performed using AT commands. See the nRF93M1 AT Commands reference guide for more information.

The following figure shows an example of the test flow in production.

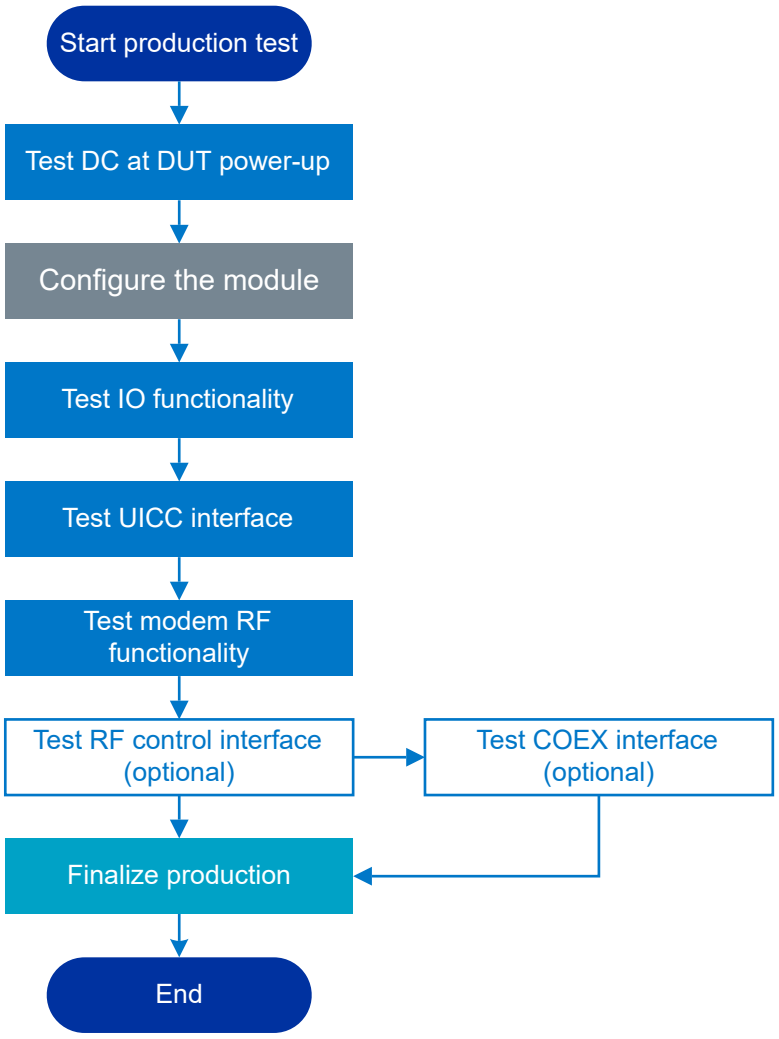

Figure 9: Example of test flow in production

6.1 Test DC at DUT power-up

If test points are available for measurement, voltage levels can be obtained from the **VDD** and **LDO_OUT** pins.

Expected values for these parameters are shown in Table 8: Voltage levels of **VDD** and **LDO_OUT** on page 32.

6.2 Configure the module

Configure the nRF93M1 with AT commands. Configuration can include for example `%MODULECFG` definitions and antenna tuner configurations.

For AT commands and configuration options, refer to the nRF93M1 AT Commands reference guide.

6.3 Test IO functionality

If the end product uses the **NETWORK** pin or the **STATUS** pin, they can be tested by measuring the pin's state from a dedicated test point. If the pins are connected to LEDs, the functionality can also be monitored by the state of the corresponding LED.

6.4 Test UICC interface

To test *UICC* functionality, turn on the SIM interface and read the *International Mobile Subscriber Identity (IMSI)*.

```
AT+CFUN=4
OK
AT+CIMI
<IMSI>
```

See the nRF93M1 AT Commands reference guide for more information.

6.5 Test modem RF functionality

nRF93M1 is fully calibrated and does not require any additional RF calibration. It is enough to verify successful assembly and soldering. For this purpose, nRF93M1 supports the Nordic-proprietary **%RFTEST** RF test AT command.

To confirm the LTE RF functionality, usually testing either TX or RX is enough.

The support for the AT command-based test mode is intended for non-signaling RF testing and allows the use of lower cost test equipment, such as a spectrum analyzer and RF signal generator. The following figures show alternative setups for RF testing.

In the setups shown in the following figures, the RF attenuator is intended to stabilize RF impedance seen by the nRF93M1 antenna port due to test fixture and cabling. For example, an attenuator of 6 dB to 10 dB can be used.

The setup in the following figure supports only RX RSSI testing.

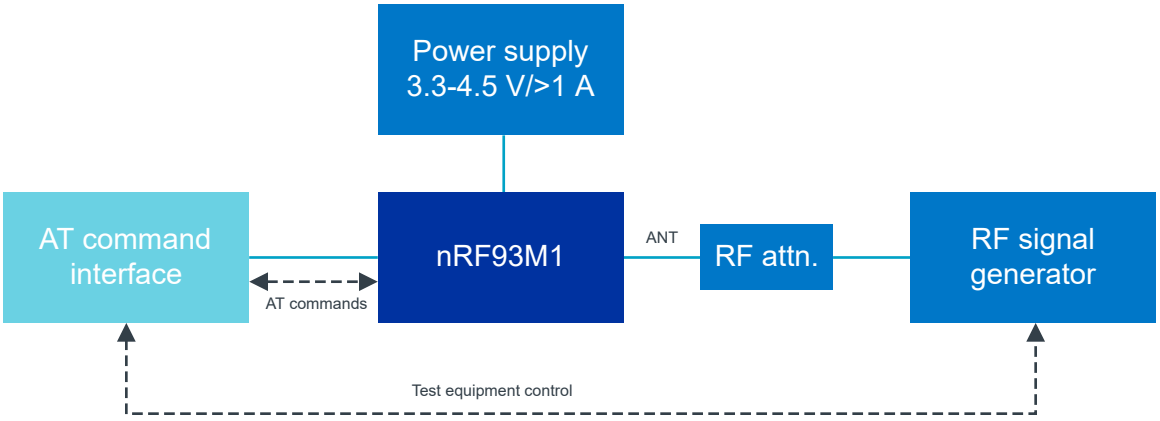

Figure 10: Non-signaling RF test setup for LTE RX RSSI mode testing

The following command example performs an RX RSSI test on band 3 at 1825.0 MHz with 15 MHz bandwidth. See the nRF93M1 AT Commands reference guide for more information.

```
AT+CFUN=0
OK
AT%RFTEST=0,1
OK
MT000000000000

AT%RFTEST=2,1,3,18250,4
OK
MT00000040050FCFFFF0000

AT%RFTEST=0,0
OK
MT000000000000
```

The setup in the following figure contains a non-signaling RF test setup for LTE TX continuous wave testing. See the nRF93M1 AT Commands reference guide for more information.

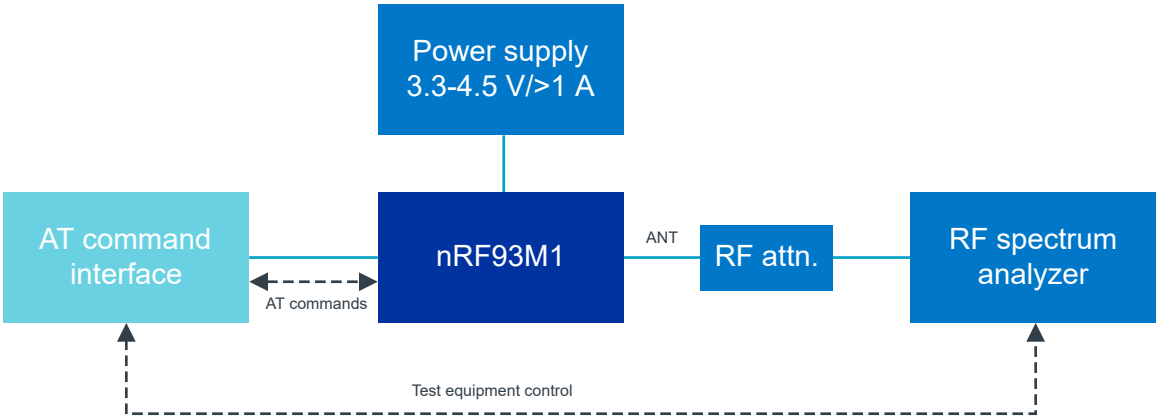

Figure 11: Non-signaling RF test setup for LTE TX testing

The following command example performs a TX single-tone test on band 5 at 836.5 MHz with 23 dBm.

```
AT+CFUN=0
OK
AT%RFTEST=0,1
OK
MT000000000000

AT%RFTEST=1,1,5,8365,23
OK
MT000000000000

AT%RFTEST=1,0
OK
MT000000000000

AT%RFTEST=0,0
OK
MT000000000000
```

For information on RF performance related test modes and other supported test capabilities, see the nRF93M1 AT Commands reference guide.

6.6 Test RF control interface

As no dedicated test commands are provided, RF control pins can be tested during non-signaling or signaling RF testing. For example, testing can be performed by measuring a pin's state from a dedicated test point during non-signaling TX or RX testing.

6.7 Test COEX interface

As no dedicated test commands are provided, the COEX interface pins can be tested during non-signaling or signaling RF testing. For example, testing can be performed by measuring a pin's state from a dedicated test point during non-signaling TX or RX testing.

6.8 Finalize production

When the production test is complete, the Nordic-proprietary `%PRODDONE` AT command must be run.

CAUTION: Running the `%PRODDONE` command prevents the end-user from modifying nRF93M1 settings.

See the nRF93M1 AT Commands reference guide for more information.

Glossary

Electromagnetic Compatibility (EMC)

A measure of how well electrical equipment coexists with its electromagnetic environment without causing or experiencing interference.

Electromagnetic Interference (EMI)

Electromagnetic noise or energy that causes disturbance and unwanted effects that interfere with the operation of an electrical circuit.

Electrostatic Discharge (ESD)

A sudden discharge of electric current between two electrically charged objects.

Embedded SIM (eSIM)

A form of programmable *SIM* that is embedded directly into a device.

Global Navigation Satellite System (GNSS)

A satellite navigation system with global coverage. The system provides signals from space transmitting positioning and timing data to GNSS receivers, which use this data to determine location.

International Mobile Subscriber Identity (IMSI)

A unique code, usually 15 digits, used for the identification of a mobile subscriber and consisting of an *Mobile Country Code (MCC)*, *Mobile Network Code (MNC)*, and MSIN (Mobile Subscription Identification Number).

Mobile Country Code (MCC)

A unique three-digit part of an IMSI code identifying the country of domicile of the mobile subscriber. MCC is used together with the Mobile Network Code (MNC).

Mobile Network Code (MNC)

A code identifying the telecommunications network. The code is defined by ITU-T Recommendation E.212, consists of two or three decimal digits, and is used together with the Mobile Country Code (MCC).

Microcontroller Unit (MCU)

A small computer on a single metal-oxide-semiconductor integrated circuit chip.

Integrated Circuit (IC)

A semiconductor chip consisting of fabricated transistors, resistors, and capacitors.

Internet of Things (IoT)

Physical objects that are embedded with sensors, processing ability, software, and other technologies that connect and exchange data with other devices and systems of the Internet or other communications networks.

Long-Term Evolution (LTE)

A wireless broadband communication standard for mobile devices and data terminals, based on the GSM/EDGE and UMTS/HSPA technologies.

Power Amplifier (PA)

A device used to increase the transmit power level of a radio signal.

Printed Circuit Board (PCB)

A board that connects electronic components.

Subscriber Identity Module (SIM)

A card used in User Equipment (UE) containing data for subscriber identification.

Switched-Mode Power Supply (SMPS)

A power supply that uses switching regulators to convert electrical power efficiently. SMPS circuits can generate wideband noise that may cause electromagnetic interference.

System on Chip (SoC)

A microchip that integrates all the necessary electronic circuits and components of a computer or other electronic systems on a single integrated circuit.

Universal Asynchronous Receiver/Transmitter (UART)

A hardware device for asynchronous serial communication between devices.

Transient Voltage Suppressor (TVS)

A protection device that clamps voltage spikes and provides a low-impedance path to ground during transient events such as electrostatic discharge.

User Equipment (UE)

Any device used by an end-user to communicate. The UE consists of the Mobile Equipment (ME) and the Universal Integrated Circuit Card (UICC).

Universal Integrated Circuit Card (UICC)

A new generation Subscriber Identity Module (SIM) used in User Equipment (UE) for ensuring the integrity and security of personal data.

Universal Subscriber Identity Module (USIM)

A card used in *User Equipment (UE)* containing data for subscriber identification.

Recommended reading

In addition to the information in this document, you might need to consult other documents.

Information related to the integration of nRF93M1 is provided in the following documents:

- nRF93M1 Preliminary Datasheet
- nRF93M1 AT Commands reference guide
- nRF93M1 DK Hardware User Guide

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