

# nPM1300

## Revision 2

**Errata**

v1.1

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# 1 nPM1300 Revision 2 Errata

This Errata document contains anomalies and configurations for the nPM1300 PMIC, Revision 2 (CAAA-D00, QEAA-D00).

The document indicates which anomalies are fixed, inherited, or new compared to [Engineering E](#).

## 2 Revision history

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nPM1300 Revision 2 v1.1	21.10.2025	<ul style="list-style-type: none"><li>• Added: No. 40. "Voltage drops on VINLDO1 or VINLDO2 at LDO startup"</li><li>• Added: No. 41. "LDO startup might cause reset"</li></ul>
nPM1300 Revision 2 v1.0	07.03.2025	<ul style="list-style-type: none"><li>• Added: No. 27. "Programming BUCK voltage increases current consumption"</li><li>• Added: No. 28. "BUCK mode transition is outside of specification"</li><li>• Added: No. 38. "LDO startup time exceeds specification "</li></ul>

# 3 New and inherited anomalies

The following anomalies are present in Revision 2 of the nPM1300 PMIC.

ID	Module	Description	Inherited from Engineering E
27	BUCK	Programming BUCK voltage increases current consumption	X
28	BUCK	BUCK mode transition is outside of specification	X
38	LOADSW/LDO	LDO startup time exceeds specification	X
40	LOADSW/LDO	Voltage drops on VINLDO1 or VINLDO2 at LDO startup	X
41	LOADSW/LDO	LDO startup might cause reset	X

Table 1: New and inherited anomalies

## 3.1 [27] BUCK: Programming BUCK voltage increases current consumption

This anomaly applies to Revision 2, build codes CAAA-D00, QEAA-D00.

It was inherited from the previous PMIC revision [Engineering E](#).

### Symptoms

Quiescent current of BUCK is higher than expected.

### Conditions

Host software sets BUCK voltage for the first time after a power-up event, and the value is the same as the voltage already set by VSET resistor. This is done by setting BUCKnSWCTRLSEL to SWCTRL while BUCKnNORMVOUT and BUCKnVOUTSTATUS are equal.

### Consequences

BUCK quiescent current increases by 1 mA.

### Workaround

Host software must initially ensure BUCKnNORMVOUT and BUCKnVOUTSTATUS are not equal when BUCKnSWCTRLSEL is set. Host software can set BUCKnNORMVOUT equal to BUCKnVOUTSTATUS once an alternate BUCKnNORMVOUT has been set.

## 3.2 [28] BUCK: BUCK mode transition is outside of specification

This anomaly applies to Revision 2, build codes CAAA-D00, QEAA-D00.

It was inherited from the previous PMIC revision [Engineering E](#).

### Symptoms

BUCK changes mode from Hysteretic to PWM or from PWM to hysteretic at a load current that deviates from typical specification. Increased output voltage ripple or increased quiescent current might be seen as a result of this.

### Conditions

BUCK is enabled in AUTO mode. When input voltage is above 4.2 V and output voltage is set below 1.4 V, PWM to Hysteretic transition level has an increased spread. For high input voltages and high output voltages, Hysteretic to PWM transition can happen at a lower load current than expected.

### Consequences

When BUCK is in PWM instead of being in Hysteretic mode, BUCK quiescent current can increase by approximately 4 mA causing lower efficiency at light load currents. When BUCK is toggling between PWM and Hysteretic modes, increased output voltage ripple might be observed.

### Workaround

Force hysteretic or PWM mode through TWI or through a configured GPIO from host software. Choose mode to maximize efficiency.

## 3.3 [38] LOADSW/LDO: LDO startup time exceeds specification

This anomaly applies to Revision 2, build codes CAAA-D00, QEAA-D00.

It was inherited from the previous PMIC revision [Engineering E](#).

### Symptoms

LDO startup duration is significantly longer than the  $t_{SS}$  typical value stated in LOADSW/LDO Electrical specification.

### Conditions

The LDO is enabled when BUCKs are disabled or BUCKs have no load and there is no active TWI communication.

### Consequences

LDO output voltage slowly rises to the configured  $V_{OUT\_LDO}$ .

## Workaround

After enabling the LDO, trigger any TWI command.

## 3.4 [40] LOADSW/LDO: Voltage drops on VINLDO1 or VINLDO2 at LDO startup

This anomaly applies to Revision 2, build codes CAAA-D00, QEAA-D00.

It was inherited from the previous PMIC revision [Engineering E](#).

### Symptoms

LDO input voltage drops.

### Conditions

LOADSW1/LDO1 or LOADSW2/LDO2 starts up in LDO mode.

### Consequences

The following can occur during the LDO startup:

- The device is powered from VBUS:
  - When the LDO input is connected to VSYS and VBUSINILIM0 is set to 100 mA, VSYS can drop to VBAT level and the charger can enter supplement mode.
  - When BUCK is used in forced PFM mode and BUCK output is used as the LDO input, the voltage on BUCK output might drop more than 1 V.
- The device is powered from VBAT:
  - When the LDO input is connected to VSYS and VBAT is less than  $V_{OUT} + V_{DROPOUT} + 300$  mV, BUCK converter can go to drop-out and out of regulation.
  - When BUCK is used in forced PFM mode and BUCK output is used as the LDO input, the voltage on BUCK output might drop more than 1 V.

**Note:** Starting up both LDOs within 200  $\mu$ s of each other increases the impact of the described consequences.

## Workaround

Apply the appropriate workaround:

- When the device is powered from VBUS and LDO input is connected to VSYS, increase the VBUSINILIM0 limit to 500 mA or higher before enabling LDO to reduce the voltage drop.
- When BUCK output is used as the LDO input, use BUCK in PWM mode or automatic mode.
- Avoid starting up both LDOs within 200  $\mu$ s of each other.

## 3.5 [41] LOADSW/LDO: LDO startup might cause reset

This anomaly applies to Revision 2, build codes CAAA-D00, QEAA-D00.

It was inherited from the previous PMIC revision [Engineering E](#).

**Symptoms**

The device resets at LDO startup due to voltage drop on VBAT.

**Conditions**

The device is powered from VBAT, and LDO is supplied by VSYS. VBAT voltage level is less than 300 mV above  $VSYS_{POF}$  when starting up LOADSW1/LDO1 or LOADSW2/LDO2 in LDO mode.

**Consequences**

The device resets, and LDO does not start up.

**Workaround**

Ensure that  $VSYS_{POF}$  is set to at least 300 mV below the minimum VBAT before starting LDO.