

Product Anomaly Notification (PAN)

Device affected (product name): nRF24LU1	Device version(s) affected: Build code CX
Date (YYYY-MM-DD): 2007-08-17	PAN no.: PAN-006
Nordic Semiconductor reference: Thomas Embla Bonnerud	Document version: 1.0

Summary

Anomalies:

1. USB OUT transactions sometimes causes the USB hardware to fail, resulting in no response from the nRF24LU1 device.
2. Not possible to use PDATA external memory addressing.
3. SMISO not high impedance when SSCN is high.

Marking / tracing:

Affected devices:

N	R	F		C	X
2	4	L	U	1	
0	7	-	-	-	-

Authorization for Nordic Semiconductor


Product Manager

Date:

Sign:

Thomas E. Bonnerud

17.08.2007



Detailed Description

Anomaly #1
Symptoms: USB OUT transactions sometimes causes the USB hardware to fail, resulting in no response from the nRF24LU1 device.
Conditions: Problem is timing related and disappears at low temperatures.
Consequences: USB compliance is not acceptable.
Workaround: <i>Alternative 1:</i> Use a 22pF capacitor from D+ to ground. This compensates marginal internal timing so that nRF24LU1 USB hardware works properly under all conditions. <i>Alternative 2:</i> nRF24LU1 without this anomaly will be available by early November 2007.

Anomaly #2
Symptoms: Not possible to use PDATA external memory addressing.
Conditions: When using the "compact memory model" for variables and accessing these by MOVX @Rn instructions the correct physical memory will not respond.
Consequences: Some manual speed optimization by declaring certain variables as PDATA is lost.
Workaround: In the <i>compiler</i> do NOT use Compact Memory Model, only Small and Large. Make sure no variable is declared as a PDATA variable. Do NOT use the MOVX @Rn assembly instruction.

Anomaly #3
Symptoms: SMISO not high impedance when SSCN is high.
Conditions: nRF24LU1 used as a SPI slave in a SPI multipoint bus with more than one slave.
Consequences: SPI buses with more than one slave will be inefficient.
Workaround: <i>Alternative 1:</i> Use an external tri-state buffer for SMISO. <i>Alternative 2:</i> Handle SMISO tri-state control from firmware. <ol style="list-style-type: none">1. Enable SCSN by clearing bits 4 and 5 in SSCONF register2. In SPI interrupt routine<ol style="list-style-type: none">a. Set P0DIR.2 = 1 when SSSTAT.2 is 1b. Set P0DIR.2 = 0 when SSSTAT.1 is 1 Will slow down every SPI bus transaction involving the nRF24LU1. Host will have to compensate for interrupt latency before starting to clock in a command to nRF24LU1, and compensate for interrupt latency before addressing the next device after the nRF24LU1 has been used.